CSE-210-F COMPUTER ARCHITECTURE & ORGANIZATION

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3 1 0

Class Work Marks: 50
Exam Marks: 100
Total Marks: 150
Duration of Exam: 3 Hrs.

NOTE: For setting up the question paper, question no 1 will be set up from all the four sections which will be compulsory and of short answer type. Two questions will be set from each of the four sections. The students have to attempt first common question, which is compulsory, and one question from each of the four sections. Thus students will have to attempt 5 questions out of 9 questions.

Section A

Boolean algebra and Logic gates, Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder), Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept, Flynn's classification of computers (SISD, MISD, MIMD); Multilevel viewpoint of a machine: digital logic, micro architecture, ISA, operating systems, high level language; structured organization; CPU, caches, main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.

Section B: Instruction Set Architecture

Instruction set based classification of processors (RISC, CISC, and their comparison); addressing modes: register, immediate, direct, indirect, indexed; Operations in the instruction set; Arithmetic and Logical, Data Transfer, Control Flow; Instruction set formats (fixed, variable, hybrid); Language of the machine: 8086 ; simulation using MSAM.

Section C: Basic non pipelined CPU Architecture and Memory Hierarchy & I/O Techniques

CPU Architecture types (accumulator, register, stack, memory/ register) detailed data path of a typical register based CPU, Fetch-Decode-Execute cycle (typically 3 to 5 stage); microinstruction sequencing, implementation of control unit, Enhancing performance with pipelining. The need for a memory hierarchy (Locality of reference principle, Memory hierarchy in practice: Cache, main memory and secondary memory, Memory parameters: access/ cycle time, cost per bit); Main memory (Semiconductor RAM & ROM organization, memory expansion, Static & dynamic memory types); Cache memory (Associative & direct mapped cache organizations.

Section D: Introduction to Parallelism and Computer Organization [80x86]

Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law; Instruction level parallelism (pipelining, super scaling –basic features); Processor level parallelism (Multiprocessor systems overview).

Instruction codes, computer register, computer instructions, timing and control, instruction cycle, type of instructions, memory reference, register reference. I/O reference, Basics of Logic Design, accumulator logic, Control memory, address sequencing, micro-instruction formats, micro-program sequencer, Stack Organization, Instruction Formats, Types of interrupts; Memory Hierarchy.

TEXT BOOKS:

1. Computer Organization and Design, 2nd Ed., by David A. Patterson and John L. Hennessy, Morgan 1997, Kauffmann.
2. Computer Architecture and Organization, 3rd Edi, by John P. Hayes, 1998, TMH.

REFERENCE BOOKS:

1. Operating Systems Internals and Design Principles by William Stallings,4th edition, 2001, Prentice-Hall Upper Saddle River, New Jersey
2. Computer Organization, 5th Edi, by Carl Hamacher, Zvonko Vranesic,2002, Safwat Zaky.
3. Structured Computer Organisation by A.S. Tanenbaum, 4th edition, Prentice-Hall of India, 1999, Eastern Economic Edition.
4. Computer Organisation & Architecture: Designing for performance by W. Stallings, 4th edition, 1996, Prentice-Hall International edition.
5. Computer System Architecture by M. Mano, 2001, Prentice-Hall.
6. Computer Architecture- Nicholas Carter, 2002, T.M.H.