EE-330-F DIGITAL SYSTEM DESIGN LAB

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CLASS WORK	:	25 Marks
EXAM	:	25 Marks
TOTAL	:	50 Marks

DURATION OF EXAM : 3 HRS

List Of Experiments:

1. Design all gates using VHDL.
2. Write VHDL programs for the following circuits, check the wave forms and the hardware generated
   a. half adder
   b. full adder
3. Write VHDL programs for the following circuits, check the wave forms and the hardware generated
   a. multiplexer
   b. demultiplexer
4. Write VHDL programs for the following circuits, check the wave forms and the hardware generated
   a. decoder
   b. encoder
5. Write a VHDL program for a comparator and check the wave forms and the hardware generated
6 Write a VHDL program for a code converter and check the wave forms and the hardware generated
7. Write a VHDL program for a FLIP-FLOP and check the wave forms and the hardware generated
8. Write a VHDL program for a counter and check the wave forms and the hardware generated
9. Write VHDL programs for the following circuits, check the wave forms and the hardware generated
   a. register
   b. shift register
10. Implement any three (given above) on FPGA/CPLD kit

Note :

Ten experiments are to be performed out of which at least seven experiments should be performed from above list. Remaining three experiments may either be performed from the above list or designed & set by the concerned institution as per the scope of the syllabus.